REMARKS

In view of the foregoing amendments and the following remarks, reconsideration and allowance are requested.

Claims 28-29 are rejected under 35 U.S.C. 112 for allegedly being indefinite.

Claim 11 was rejected under 35 U.S.C. 102(b) for allegedly being anticipated by U.S. Patent No. 6,407,591 to Wong et. al. ("Wong"). Wong was not published within 1 year of the filing date of the current disclosure, the Examiner modified this rejection in a phone call on December 3, 2003 by changing the ground for the rejection to 35 U.S.C. 102(a).

Claims 9, 22-23 were rejected under 35 U.S.C. 103(a) for allegedly being anticipated by Wong. Under a section entitled "*Claim Rejections - 35 U.S.C. 103*" in the Office Action, Claims 9, 22-23 were said to be rejected under 35 U.S.C. 102(b) to Wong. The Examiner stated in a phone call on December 3, 2003 that these claim rejections were mislabeled in the Office Action and should be 35 U.S.C. 103(a) rejections instead.

Claims 1-5, 7-8, 12-15, 20-21 and 27-29 were rejected under 35 U.S.C. 103(a) for allegedly being anticipated by Wong in view of U.S. Patent No. 5,557,242 to Wetherell. Under the section entitled "*Claim Rejections - 35 U.S.C. 103*" in the Office Action, Claims 1-5, 7-8, 12-15, 20-21 and 27-29 were said to be rejected under 35 U.S.C. 102(e) to Wong and Wetherell. The Examiner stated in a phone call on December 3, 2003 that these claim rejections were mislabeled in the Office Action and should be 35 U.S.C. 103(a) rejections instead.

Claim 30 has been allowed.

Claims 1-5, 7-9, 11-15, 20-23, and 27-29 are pending, with claims 1, 4, 9, 11, 20, 22, 27-29 being independent.

Applicant respectfully traverses the rejections, and requests reconsideration and allowance.

35 U.S.C. 112 Rejection for Claims 28-29

Claim 28

Claim 28 is definite at least because the claim pointed out and distinctly claimed the subject matter which the applicants regarded as their invention. The specification provides support for the claimed subject matter.

For example, see the claimed subject matter described in reference to Figures 3 and 4a in the disclosure. The first input terminal is CLK# (18), and the second input terminal is CLK (16). The clock generator "issues one of a single-ended clock signal or a differential clock signal" to the electronic device (40). The clock generator (page 17, lines 1-4) supplies the master clock signal to the electronic device (40). The device can generate "a single-ended clock signal of the same frequency as the clock signal issued by the clock generator" as shown in reference to HCLK 62 (page 5, lines 9-20).

Fig. 4a shows a case in which the electronic device (40) receives a single-ended signal from the clock generator. The first input terminal (18) is at a "constant ground potential" (p.6, lines 4-5). Furthermore, the timing diagram in Figure 4a shows that CLK# is constant (page 10, lines 4-9). Hence, the elements of Claim 28 are distinctly described in the disclosure.

Because Claim 28 at least points out and claims the subject matter within the disclosure, the 35 U.S.C. 112 rejection should be withdrawn and Claim 28 should be placed in condition for allowance.

Claim 29

Claim 29 is definite at least because the claim pointed out and distinctly claimed the subject matter which the applicants

regarded as their invention. The specification provides support for the claimed subject matter.

For example, see the claimed subject matter described in reference to Figures 3 and 4b in the disclosure. The first input terminal is CLK# (18), and the second input terminal is CLK (16). The clock generator "issues one of a single-ended clock signal or a differential clock signal" to the electronic device (40). The clock generator (page 17, lines 1-4) supplies the master clock signal to the electronic device (40). The device can generate "a single-ended clock signal of the same frequency as the clock signal issued by the clock generator" as shown in reference to HCLK 62 (page 5, lines 9-20).

Fig. 4b shows a case in which the electronic device (40) receives a differential-ended signal from the clock generator. Claim 29 has been amended to clearly convey that " the electronic device receives a clock signal at the first terminal and a clock signal at the second terminal that are one hundred eighty degrees out of phase" (page 11, lines 9-12). The timing diagram in Figure 4b clearly shows that CLK# and CLK are one hundred eighty degrees out of phase, and Figure 3 clearly shows that CLK# and CLK are the input signals of the electronic device (40). Hence, the features of Claim 29 are clearly described in the disclosure.

Because Claim 29 at least distinguishes and claims the subject matter within the disclosure, the 35 U.S.C. 112 rejection should be withdrawn and Claim 29 should be placed in condition for allowance.

35 U.S.C. 103 Rejections

Claims 1-5, 7-9, 12-15, 20-23 and 27-29 are allowable at least because the Wong reference and the present disclosure are commonly owned (by Intel Corporation).

Section 2136.02 of the MPEP states the following:

> For applications filed on or after November 29, 1999, if the applicant provides evidence that the application and prior art reference were owned by the same person, or subject to an obligation of assignment to the same person, at the time the invention was made, any rejections under 35 U.S.C. 102(e)/ 103 based upon such a commonly owned reference should not be made or maintained.

Therefore, the 35 U.S.C. 103 rejection to Claims 1-5, 7-9, 12-15, 20-23 and 27-29 should be withdrawn and those claims should be allowed.

35 U.S.C. 102(a) - Claim 11

Claim 11 is patentable over Wong at least because Wong does not anticipate at least one feature of the claim. For instance, Wong fails to anticipate a detector "configured to output a clock mode signal as a function of a voltage potential of the second clock signal." Wong only shows one output to the device in Figures 2 and 3. In Figure 2, Wong only shows the output of the MUX 217, and in Figure 3, Wong only shows the output of CSDA. In each figure, the output of the device is not an output clock mode signal that is a function of a voltage potential of the second clock signal. Therefore, Wong fails to teach such a feature.

Not only does Wong fail to show an output clock mode signal, Wong does not teach how such an output clock mode signal can be used in conjunction with aligning the output signal of the device with the signal from the clock generator. Therefore, Wong fails to teach a functional use of the output clock mode signal that is taught in the current disclosure.

Since Wong does not anticipate at least one feature of the claim, then the 102(a) rejection to Claim 11 should be withdrawn and that claim should be allowed.

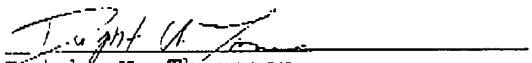
Conclusion

In view of the amendments and remarks herein, Applicants believe that Claims 1-5, 7-9, 11-15, 20-23 and 27-29 are in condition for allowance and ask that those pending claims be allowed. The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, Applicants' arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

No fee is believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 12/05/03



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